CLAIMS

What is claimed is:

1. An integrated circuit device for communicating with a first tester of a first pin capacity to receive test vectors developed for a second tester of a second pin capacity, said device comprising:

scan chains; and

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on a mode signal, said reconfiguration logic providing compatibility between said test vectors and said second tester having said second pin capacity, said mode signal selecting between said first tester and said second tester.

2. A device as described in Claim 1 wherein said second pin capacity is less than said first pin capacity.

3. A device as described in Claim 2 wherein said second pin capacity is approximately more than 64 pins and said first pin capacity is approximately more than 1000 pins.

4. A device as described in Claim 1 wherein said reconfiguration logic comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

5. A device as described in Claim 1 wherein said reconfiguration logic comprises:

a functional input shift register for receiving functional inputs and used for a mode corresponding to said tester of said second pin capacity; and

a functional output shift register for providing functional output values and used for said mode corresponding to said second pin capacity.

6. A device and described in Claim 5 wherein said reconfiguration logic also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said mode signal.

7. A device as described in Claim 1 further comprising a protocol unit coupled to said mode signal and comprising a first test sequence used for said tester of said first pin capacity and containing a second test sequence used for said tester of said second pin capacity.

8. An automated testing equipment (ATE) system for testing an integrated circuit device comprising:

a storage medium for storing a set of test vectors developed for a tester having a first pin capacity;

a user selector selecting modes between a tester having said first pin capacity and a tester having a second pin capacity; and

a device under test for coupling with one of said testers to receive said test vectors, said device under test comprising:

scan chains; and

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on said user selector, said reconfiguration logic providing compatibility between said test vectors and said tester having said second pin capacity.

9. A system as described in Claim 8 wherein said second pin capacity is less than said first pin capacity.

10. A system as described in Claim 9 wherein said second pin capacity is approximately more than 64 pins and said first pin capacity is approximately more than 1000 pins.

11. A system as described in Claim 8 wherein said reconfiguration logic comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

12. A system as described in Claim 8 wherein said reconfiguration logic of said device under test comprises:

a functional input shift register for receiving functional inputs and used for a mode corresponding to said tester of said second pin capacity; and

a functional output shift register for providing functional output values and used for said mode corresponding to said second pin capacity.

13. A system and described in Claim 12 wherein said reconfiguration logic of said device under test also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said user selector.

14. A system as described in Claim 8 further comprising a protocol unit coupled to said user selector and comprising a first test sequence used for said tester of said first pin capacity and containing a second test sequence used for said tester of said second pin capacity.

15. An automated testing equipment (ATE) system for testing an integrated circuit device comprising:

a storage medium for storing a set of test vectors developed for a tester having a high pin capacity;

a selector operable to select a test mode between a tester having said high pin capacity and a tester having a low pin capacity; and

a device under test for coupling with one of said testers to receive said test vectors, functional input values and said test mode and for coupling to provide test results, said device under test comprising:

scan chains; and

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on said test mode, said reconfiguration logic providing compatibility between said test vectors and said tester having said low pin capacity.

16. A system as described in Claim 15 wherein reconfiguration logic decreases the number of pins required to test said device under test for a test mode that is used for said tester having said low pin capacity

17. A system as described in Claim 15 wherein said low pin capacity is approximately more than 64 pins and said high pin capacity is approximately more than 1000 pins.

18. A system as described in Claim 15 wherein said reconfiguration logic comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

19. A system as described in Claim 15 wherein said reconfiguration logic of said device under test comprises:

a functional input shift register for receiving functional inputs and used for a test mode corresponding with said tester of said low pin capacity; and

a functional output shift register for providing functional output values and used for said test mode corresponding with said low pin capacity.

20. A system and described in Claim 19 wherein said reconfiguration logic of said device under test also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said test mode.

21. A system as described in Claim 15 further comprising a protocol unit coupled to said user selector and comprising a first test sequence used for said tester of said high pin capacity and containing a second test sequence used for said tester of said low pin capacity.

22. In an automated testing equipment (ATE) system having a device to be tested, a method for testing said device comprising the steps of:

a) storing, in a storage medium, a set of test vectors developed for a tester having a first pin capacity;

b) selecting a test mode as between a tester having said first pin capacity and a tester having a second pin capacity; and

c) in response to said step b), altering the number of pins required to test said device under test by reconfiguring the individual length and number of scan chains internal to said device based on said test mode, wherein said altering provides compatibility between said test vectors and said tester having said second pin capacity.

23. A method as described in Claim 22 further comprising the step of d) applying said test vectors to said device under test using said tester having said second pin capacity.

24. A method as described in Claim 23 wherein said second pin capacity is less than said first pin capacity.

25. A method as described in Claim 24 wherein said second pin capacity is approximately more than 64 pins and said first pin capacity is approximately more than 1000 pins.

26. A method as described in Claim 23 wherein said step c) is performed by reconfiguration logic that comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

27. A method as described in Claim 26 wherein said reconfiguration logic of said device under test also comprises:

a functional input shift register for receiving functional inputs and used for a test mode corresponding with said tester of said second pin capacity; and

a functional output shift register for providing functional output values and used for said test mode corresponding with said second pin capacity.

28. A method as described in Claim 27 wherein said reconfiguration logic of said device under test also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said test mode selected.

29. A method as described in Claim 23 wherein said step d) further comprises the steps of:

d1) applying a first test sequence used for said tester of said first pin capacity; and

d2) applying a second test sequence used for said tester of said second pin capacity.